DESIGN NOTES

A Robust 10MHz Reference Clock Input Protection Circuit and Distributor for RF Systems – Design Note 514

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Introduction

Designing the reference input circuit for an RF system can prove tricky. One challenge is maintaining the phase noise performance of the input clock while meeting the protection, buffering and distribution requirements for the clock. This article shows how to design a 10MHz reference input circuit and optimize its performance.

Design Requirements

RF instruments and wireless transceivers often feature an input for an external reference clock, such as the ubiquitous 10MHz reference input port found on RF instruments. Many of these same systems include a provision to distribute the reference clock through the system. Figure 1 shows a common scheme, where the reference clock supplies the reference input to two distinct phase-locked loops (PLLs).

A well-designed, robust input would accept both sine and square wave signals over a wide range of amplitudes. It would maintain a constant signal level drive to the destination PLL inputs inside the system, even in the face of varied inputs. The exposed-to-the-world reference input port should have overvoltage/overpower protection. Most importantly, the inevitable degradation in the phase noise performance of the clock signal should be minimized.

Design Implementation

The LTC®6957 is a very low additive phase noise (or jitter) dual-output clock buffer and logic translator. The input of the LTC6957 accepts a sine or a square wave over a wide range of amplitudes and drives loads at constant amplitude.
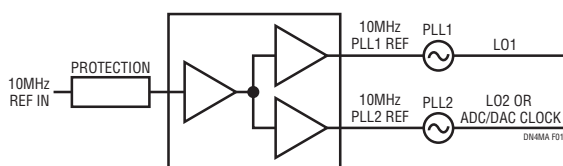
Figure 1. Block Diagram of a Common Reference Input and Reference Distribution for an RF System

The LTC6957 offers various output logic signal options: PECL, LVDS and CMOS (in-phase and complementary), allowing it to drive a wide range of loads. Figure 2 shows a 10MHz reference input circuit using the LTC6957-3, which produces two in-phase CMOS outputs.

The transformer shown in Figure 2 serves several functions. First, in conjunction with the Schottky diodes following it, it offers input overpower/overvoltage protection. The diodes limit the AC voltage seen by the LTC6957-3. The WBC16-1T can handle up to 0.25W power ($3.5V_{RMS}$ into 50Ω).

The transformer also isolates the connector ground—which is usually tied to the chassis of the RF system—from the internal analog ground of the system.

Furthermore, the transformer applies a voltage gain to the incoming signal, thus steepening the edges seen by the LTC6957-3. This helps reduce AM-to-PM noise conversion, which in turn limits phase noise degradation, especially with small input signals. The WBC16-1T has a voltage gain of four. It is possible to rely on the transformer's voltage gain of four, as opposed to its maximum and ideal power gain of one, because the LTC6957-3 presents a high impedance load to the transformer.

R1 and R2 can be adjusted in combination to match the input port to 50Ω. For small input signals, the diodes are off and the transformer sees a load of 804Ω in Figure 2. That load is reflected to the input as approximately 50Ω because of the transformer's primary-to-secondary impedance ratio of 16. For larger input signals, the Schottky diodes turn on, reducing the 604Ω resistance to nearly a short circuit. This degrades the reference input return loss—a problem that can be avoided by adjusting the values of R1 and R2, but there are trade-offs to doing so.

For large input signals, the input return loss can be improved by increasing R1's value, and reducing R2's
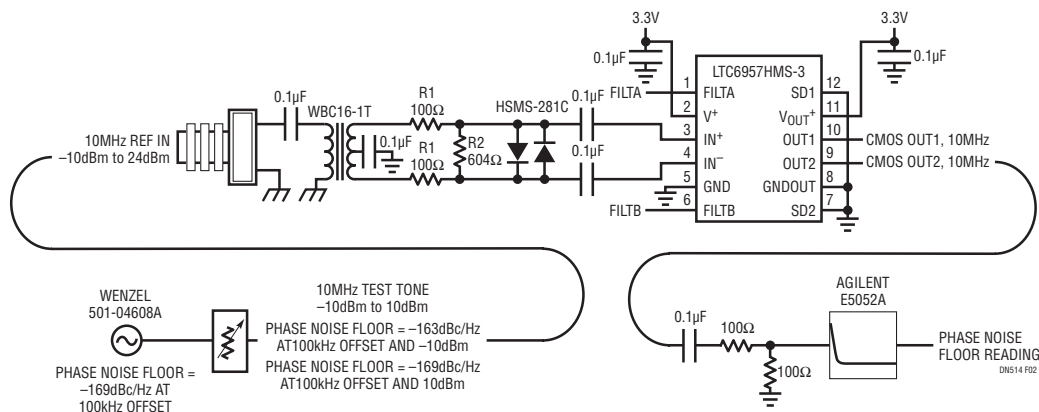
Figure 2. 10MHz Reference Input Circuit Employing the LTC6957-3 with Front-End Protection, Shown with Test Signal and Phase Noise Measurement Set-Up

value, such that their combined series resistance remains around 800Ω. However, since R1 appears in series with the signal, it adds noise to it. A larger R1 comes in combination with a smaller R2, resulting in a smaller portion of the signal appearing at the LTC6957-3's input, further degrading the phase noise performance. In other words, the designer can trade off phase noise performance for input return loss by playing with the values of R1 and R2. The values shown in Figure 2 strike an overall balance of these two performance metrics.

The AC-coupling capacitor separating the connector from the transformer in Figure 2 offers input protection from DC sources.

The LTC6957-3 has internal lowpass filters that can be selected via the FILTA and FILTB pins. This option strategically limits the bandwidth of the LTC6957's first amplifier stage, and hence, the additive phase noise of the circuit, especially when the input signal is weak as shown below.
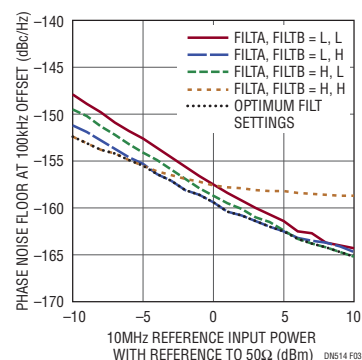
Performance

A 10MHz OCXO is connected to the input of the circuit via a step attenuator as shown in Figure 2. The reference input signal is varied between –10dBm and 10dBm while measuring the phase noise floor at the output of the LTC6957-3 with different input filter settings using the Agilent E5052A signal source analyzer. Figure 3 shows the phase noise floor of the 10MHz CMOS clock output of the LTC6957-3 measured at a 100kHz offset.

If the amplitude of the externally applied 10MHz reference signal is not known, pulling FILTA low and FILTB high yields good overall phase noise performance as shown in Figure 3. Nevertheless, performance can be optimized if the applied signal level at the input is measured and appropriate filter settings are applied.

The R1 and R2 values chosen in Figure 2 result in an input return loss of –9dB when the reference input's power is 0dBm into 50Ω. The return loss is better at lower input powers and worse at higher powers.

Figure 3. 100kHz Offset Phase Noise Floor at the Output of the LTC6957-3 vs 10MHz Reference Input Power Level for Various LTC6957 Filter Settings

Conclusion

A robust, high performance 10MHz reference input circuit is built around the LTC6957-3. Features include a wide range of input signal type and level compatibility, protection and clock distribution with limited phase noise degradation. The circuit's phase noise and input return loss are evaluated and optimized. The LTC6957-3 simplifies the design process while achieving excellent overall performance.

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